



COPY OF PAPERS
ORIGINALLY FILED

2325
PATENT

Case Docket No. ASMMC.006AUS

Date: July 3, 2002

Page 1

In re application of : Raaijmakers et al.

App. No. : 09/452,844

Filed : December 3, 1999

For : CONFORMAL THIN FILMS
OVER TEXTURED
CAPACITOR ELECTRODES

Examiner : R. Rocchegiani

Art Unit : 2825

I hereby certify that this correspondence and all marked attachments
are being deposited with the United States Postal Service as first
class mail in an envelope addressed to: United States Patent and
Trademark Office, P.O. Box 2327, Arlington, VA 22202, on

July 3, 2002

(Date)

Adeel S. Akhtar
Adeel S. Akhtar, Reg. No. 41,394

UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. Box 2327
Arlington, VA 22202

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below:

CLAIMS AS FILED						
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
Total Claims	41	—	66	= 0 ×	\$18	= \$0
Independent Claims	4	—	6	= 0 ×	\$84	= \$0
If application has been amended to contain multiple dependent claim(s), then add					\$280	= \$0
Time Extension Fee						\$0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$0

(X) Return prepaid postcard.

(X) Please charge any additional fees, including any fees for additional extension of time, or credit
overpayment to Deposit Account No. 11-1410.

Adeel S. Akhtar
Adeel S. Akhtar
Registration No. 41,394
Attorney of Record

RECEIVED
JUL 15 2002
TECHNOLOGY CENTER 280C

C

#24 Amatt
Atrial
PATENT 7/23/02

48MBIC-006AUS



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Raaijmakers et al.) Group Art Unit: 2825
Appl. No. : 09/452,844)
Filed : December 3, 1999)
For : CONFORMAL THIN FILMS)
OVER TEXTURED)
CAPACITOR ELECTRODES)
Examiner : R. Rocchegiani)

RECEIVED
JUL 15 2002
TECHNOLOGY CENTER 280C

AMENDMENT IN RESPONSE TO OFFICE ACTION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action mailed on April 9, 2002, please consider the following amendments and remarks.

IN THE CLAIMS:

Please cancel Claims 2, 31, 32 and 64-66.

Please amend Claims 1, 30, 55 and 63 are indicated below.

1. (Amended) A method of forming a capacitor in an integrated circuit, comprising:
- constructing a bottom electrode including a textured silicon layer, the textured silicon layer having hemispherical grain (HSG) morphology; and
 - depositing a high k dielectric layer directly over the textured silicon layer
- wherein depositing comprises:
- forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species; and

48